

What is claimed is:

1 1. A semiconductor integrated device, comprising:  
2 a first circuit unit to which electric power is supplied  
3 from a first power supply wiring and a second power supply wiring;  
4 a second circuit unit to which electric power is supplied  
5 from a third power supply wiring and a fourth power supply wiring;  
6 a first interface circuit unit formed in the first circuit  
7 unit; and  
8 a second interface circuit unit formed in the second  
9 circuit unit, the second interface circuit unit being configured  
10 to perform any of inputting and outputting a signal to and from  
11 the first interface circuit unit,  
12 wherein the second power supply wiring is coupled through  
13 at least a protection circuit configured to be conductive at  
14 a given voltage or above, to the fourth power supply wiring  
15 at a node.

1 2. A semiconductor integrated device, comprising:  
2 a first circuit unit to which electric power is supplied  
3 from a first power supply wiring and a second power supply wiring;  
4 a second circuit unit to which electric power is supplied  
5 from a third power supply wiring and a fourth power supply wiring;  
6 a first interface circuit unit formed in the first circuit  
7 unit; and  
8 a second interface circuit unit formed in the second  
9 circuit unit, the second interface circuit unit being configured  
10 to perform any of inputting and outputting a signal to and from  
11 the first interface circuit unit,

12            wherein the second power supply wiring is coupled to the  
13 fourth power supply wiring at a node.

1    3.    The semiconductor integrated device according to claim 1,  
2            wherein the second interface circuit unit is placed in  
3 the vicinity of the first interface circuit unit.

1    4.    The semiconductor integrated device according to claim 2,  
2            wherein the second interface circuit unit is placed in  
3 the vicinity of the first interface circuit unit.

1    5.    The semiconductor integrated device according to claim 1,  
2            wherein the first interface circuit unit and the second  
3 interface circuit unit are placed at a boundary between the  
4 first circuit unit and the second circuit unit.

1    6.    The semiconductor integrated device according to claim 5,  
2            wherein the first interface circuit unit is an interface  
3 circuit unit in a first internal circuit unit and the second  
4 interface circuit unit is an interface circuit unit in a second  
5 circuit unit, and

6            the first internal circuit unit has a larger number of  
7 elements than the second internal circuit

1    7.    The semiconductor integrated device according to claim 5,  
2            wherein the first interface circuit unit is an interface  
3 circuit unit in a first internal circuit unit and the second  
4 interface circuit unit is an interface circuit unit in a second  
5 circuit unit, and

6           the first internal circuit unit has a larger chip area  
7   than the second internal circuit

1   8.   The semiconductor integrated device according to claim 1,  
2           wherein the second interface circuit unit is coupled to  
3   the fourth wiring in the vicinity of a node for the second wiring  
4   and the fourth wiring.

1   9.   The semiconductor integrated device according to claim 8,  
2           wherein the first interface circuit unit is coupled to  
3   the second wiring in the vicinity of the node for the second  
4   wiring and the fourth wiring.

1   10.   The semiconductor integrated device according to claim  
2   1,  
3           wherein an external connection pad is coupled to the fourth  
4   wiring in the vicinity of a node for the second wiring and the  
5   fourth wiring.

1   11.   The semiconductor integrated device according to claim  
2   1,  
3           further comprising an external connection pad coupled  
4   to the fourth wiring, and  
5           wherein a node for the external connection pad and the fourth  
6   wiring is located between a node for the second interface circuit  
7   unit and the fourth wiring and a node for the second wiring  
8   and the fourth wiring.

1   12.   The semiconductor integrated device according to claim

2 1,

3        wherein the first power supply wiring is coupled to the  
4 second wiring through a second protection circuit configured  
5 to be conductive at a given voltage or above in the vicinity  
6 of a node for the second wiring and the fourth wiring.

1 13. The semiconductor integrated device according to claim

2 1,

3        wherein the first power supply wiring is coupled to the  
4 second wiring through a second protection circuit configured  
5 to be conductive at a given voltage or above, and

6        a node for the first power supply wiring and the second  
7 wiring is located between a node for the first interface circuit  
8 unit and the second wiring and a node for the second wiring  
9 and the fourth wiring.

1 14. The semiconductor integrated device according to claim

2 1,

3        wherein an external connection pad coupled to the second  
4 ground wiring, and

5        the first power supply wiring is coupled to the second  
6 ground wiring through a third protection circuit configured  
7 to be conductive at a given voltage or above, and

8        a node for the third protection circuit and the fourth  
9 wiring is located between a node for the second interface circuit  
10 unit and the external connection pad.

1 15. The semiconductor integrated device according to claim

2 14,

3            wherein the node for the second interface circuit unit  
4   and the fourth wiring is located between the node for the second  
5   wiring and the fourth wiring and the node for the fourth wiring  
6   and the external connection pad.

1   16.   The semiconductor integrated device according to claim  
2   1,

3            wherein the first power supply wiring is coupled to the  
4   second wiring through a second protection circuit configured  
5   to be conductive at a given voltage or above, and

6            the second power supply wiring is coupled to the fourth  
7   wiring through a third protection circuit configured to be  
8   conductive at a given voltage or above.

1   17.   The semiconductor integrated device according to claim  
2   1,

3            wherein each of the first interface circuit unit and the  
4   second interface circuit unit comprises a clamp element  
5   configured to protect a gate for receiving an input signal.

1   18.   The semiconductor integrated device according to claim  
2   12,

3            wherein the second wiring is coupled to the first power  
4   supply wiring through the protection circuit in a position  
5   between a node for the first interface circuit unit and the  
6   first power supply wiring, and, an external connection pad of  
7   the first power supply wiring.

1   19.   The semiconductor integrated device according to claim

2 11,

3        wherein the second protection circuit coupled between  
4 the first power supply wiring and the second wiring and the  
5 protection circuit coupled between the second wiring and the  
6 fourth wiring are formed in a single cell.

1 20. The semiconductor integrated device according to claim  
2 14,

3        wherein a node for the third protection circuit and the  
4 first power supply wiring is located between a node for the  
5 first interface circuit unit and the first power supply wiring,  
6 and, an external connection pad of the first power supply wiring.

1 21. The semiconductor integrated device according to claim  
2 11,

3        wherein the second protection circuit coupled between  
4 the first power supply wiring and the fourth wiring and the  
5 protection circuit coupled between the second wiring and the  
6 fourth wiring are formed in a single cell.

1 22. The semiconductor integrated device according to claim  
2 1,

3        wherein wiring delay between the first interface circuit  
4 unit and the second interface circuit is designed to be equal  
5 to or less than a given value.

1 23. An apparatus for designing a semiconductor integrated  
2 device, comprising the steps of:

3        specifying a first interface circuit unit to be formed

4 in a first circuit unit to which electric power is supplied  
5 from first power supply wiring;

6 specifying a second interface circuit unit to be formed  
7 in a second circuit unit to which electric power is supplied  
8 from second power supply wiring, the second interface circuit  
9 unit configured to input and/or output a signal to and from  
10 the first interface circuit unit; and

11 arranging the first interface circuit unit and the second  
12 interface circuit unit closely to each other in accordance with  
13 a predetermined placement rule.

1 24. An apparatus for designing a semiconductor integrated  
2 device, comprising the steps of:

3 specifying a first interface circuit unit to be formed  
4 in a first circuit unit to which electric power is supplied  
5 from first power supply wiring;

6 specifying a second interface circuit unit to be formed  
7 in a second circuit unit to which electric power is supplied  
8 from second power supply wiring; and

9 performing wiring design so as to reduce wiring delay  
10 between the first interface circuit unit and the second interface  
11 circuit unit in accordance with a predetermined placement rule.

1 25. The apparatus for designing a semiconductor integrated  
2 device according to claim 23,

3 wherein the step of specifying the first interface circuit  
4 unit includes the steps of:

5 modifying connection information so as to short circuit  
6 a first element having a connection terminal coupled to the

7 first power supply wiring;  
8 modifying the connection information so as to short  
9 circuit a second element having a connection terminal coupled  
10 to the second power supply wiring;  
11 providing different texts respectively to the first power  
12 supply wiring and the second power supply wiring; and  
13 specifying a node where terminals provided with the  
14 different texts are short circuited.

1 26. The apparatus for designing a semiconductor integrated  
2 device according to claim 23,  
3 wherein the step of specifying the first interface circuit  
4 unit includes the steps of:  
5 obtaining a first cell for which connection information  
6 is modified so as to short circuit a first element having a  
7 connection terminal coupled to the first power supply wiring  
8 and replacing the first element with the first cell;  
9 obtaining a second cell for which the connection  
10 information is modified so as to short circuit a second element  
11 having a connection terminal coupled to the second power supply  
12 wiring and replacing the second element with the second cell;  
13 providing different names respectively to the first power  
14 supply wiring and the second power supply wiring; and  
15 specifying a node where terminals provided with the  
16 different names are short circuited.

1 27. An apparatus for designing a semiconductor integrated  
2 device comprising the steps of:  
3 modifying connection information so as to short circuit



4 a first element having a connection terminal coupled to first  
5 power supply wiring;

6 modifying the connection information so as to short  
7 circuit a second element having a connection terminal coupled  
8 to the second power supply wiring;

9 providing different names respectively to different power  
10 pads in the first power supply wiring and the second power supply  
11 wiring;

12 specifying a node where terminals provided with the  
13 different names are short circuited; and

14 performing predetermined element modification  
15 concerning the specified node.

1 28. An apparatus for designing a semiconductor integrated  
2 device, comprising the steps of:

3 obtaining a first cell for which connection information  
4 is modified so as to short circuit a first element having a  
5 connection terminal coupled to first power supply wiring and  
6 replacing the first element with the first cell;

7 obtaining a second cell for which the connection  
8 information is modified so as to short circuit an element having  
9 a connection terminal coupled to the second power supply wiring  
10 and replacing the second element with the second cell;

11 providing different names respectively to the first power  
12 supply wiring and the second power supply wiring;

13 specifying a node where terminals provided with the  
14 different names are short circuited; and

15 performing predetermined element modification  
16 concerning the specified node.

1 29. The apparatus for designing a semiconductor integrated  
2 device according to claim 27,  
3 wherein a cell including a gate protection element is  
4 added to or replaced for the specified node.

1 30. The apparatus for designing a semiconductor integrated  
2 device according to claim 28,  
3 wherein a cell including a gate protection element is  
4 added to or replaced for the specified node.